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Identifying Worst-Case Test Vectors for Delay Failures Induced by Total Dose in Flash- based FPGA

By:

Adel Abdullah Taha Ammar

A thesis submitted in partial fulfillment of
the requirements for the degree of

Masters of Science in Electronics and
communication Engineering

The American University in Cairo

2015

Approved by _____
Chairperson of Supervisory Committee

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Program to Offer Degree _____ Authorized

Date _____

The American University in Cairo

Identifying

Worst-Case Test Vectors for Delay Failures Induced by Total Ionization Dose in Flash- based FPGA

By: Adel Abdullah Taha Ammar

Thesis Supervisor: Prof. Ahmed Abou-Auf

Department of: Electronics and Communication Engineering

ABSTRACT

A thesis presented on the effects of space radiation on the flash-based FPGA leading to failure with applying a proposed fault model to identify the worst, nominal and best-case test vectors for each. This thesis analyzed the delay failure induced in a flash-based field programmable gate array (FPGA) by a total-ionizing dose. It then identified the different factors contributing to the amount of delay induced by the total dose in the FPGA. A novel fault model for delay failure in FPGA was developed. This fault model was used to identify worst-case test vectors for delay failures induced in FPGA devices exposed to a total ionizing dose. The fault model and the methodology for identifying worst-case test vectors WCTV were validated using Micro-semi ProASIC3 FPGA and Cobalt 60 radiation facility.

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ACKNOWLEDGMENTS

The author wishes to express sincere appreciation to Professor Ahmed Abou Auf, Eng Mustafa Mahmoud, Dr. Hatem Yousry and Eng Mai El Kady for their assistance in the work presented in this thesis.

GLOSSARY

ASIC: Application specific integrated circuit

EEPROM: Electrically erasable programmable read only memory

EPROM: Electrically programmable read only memory

FGMOS: Floating gate metal oxide field effect transistor

FPGA: Field programmable gate array

GA: Genetic algorithm.

MOSFET (MOS): Metal oxide field effect transistor

STA: Static timing analyzer

TID: Total ionizing dose

VLSI: Very large scale integrated circuits

WCTV: Worst case Test vectors.

Versatile: main building block of the Proasic FPGA

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Chapter 1

INTRODUCTION

1.1 Introduction

In this thesis, the worst-case test vectors (WCTV) that can be used to induce delay and leakage current failures in combinational networks (included between flip-flops in sequential circuits) exposed to radiation are identified depending on a specific fault model used to express the defects in the cells used to implement the combinational circuit design.

When any electronic circuit is exposed to electromagnetic radiation, the threshold voltage of the transistors, the building units of any digital circuit, changes causing a significant effect on the delay, leakage current or even the logical operation of the design.

1.2 Motivation

The motivation is to identify the WCTVs for any design, which could be used as a fault detection to enhance the design by avoiding these vectors, which reveals the total functional failure of the design to the logical failure limit, which occurs at higher doses.

1.3 Problem statement

The WCTVs are not a part of interest of the other research teams working on the radiation effects on the electronic circuits except for this team, which previously investigated their effect on application specific integrated circuits (ASICs).

Identifying the WCTV of designs implemented on FPGA, which is widely used in space applications, appears as a demanding point of research and it will be investigated in this thesis.

1.4 Methodology

In this thesis, two fault models were developed. One is for calculation of the leakage current and the other is for the calculation of the propagation delay in the combinational circuits.

The search for the WCTVs were performed using a genetic algorithm (GA) then the results of the search were validated using simulation in addition to physical experiments . These experiments were performed in a gamma rays radiation unit, which uses cobalt 60 as the source of radiation.

1.5 Thesis organization

The following chapters are organized as follows: Chapter 2 will discuss the theoretical background of the radiation effects on electronic circuits, Chapter 3 will introduce the propagation delay fault model and WCTV generation while in Chapter 4 the methodology for finding delay failure is presented. The contribution results are presented in Chapter 5 and finally the thesis conclusion and the future work are in Chapter 6.

Chapter 2

RADIATION EFFECTS REVIEW

Radiation hardening is a way of making electronic components, circuits and systems immune to the damage caused by both particle radiation and high energy electromagnetic radiation which can be classified as ionizing radiation. It's really important to study the effect of it and try to solve the problems appeared due o it. Electronics used in several applications subjected to ionizing radiation such as nuclear reactors, particle accelerators ad off course space applications[14].

Products, subjected to radiation testing, are called radiation-hardened products. There are different types of testing the resultant effects of the ionizing radiation including total ionization dose (TID), enhanced low dose rate effect (ELDRS), neutron displacement damage and single event effects (SEE, SET and SEB).

2.1 Problems caused by radiation

Semiconductor components operation mostly depends on the amount of charged particles and their motion, which makes them very sensitive to radiation as the last encounters either charged particle, which change the doping of the semiconductors or high-energy waves, which changes the energy of the semiconductor particles. Both the cases affect the energy band gap of the semiconductors and interns affect the threshold voltage of the transistors [14].

This considered as electronic noise, which forms signal spikes while in case of digital circuits it can cause several types of failures starting from propagation delay failure with leakage current failure until it reaches a full logical failure at high doses or energies.

2.2 Major ionization radiation sources

- **Cosmic rays:** these rays are available in space with 85% protons , 14% alpha particles and 1% (heavy ions, x-rays and gamma-rays)

- **Solar particles :** originally from Sun and also contains high energy protons and heavy ions

- **Van Allen radiation belts :** electrons and protons with high energy **(** up to 10 Mev and 100 Mev)trapped in geomagnetic field and decreases by going further from the earth and obviously the satellites while the effect strength varies with the position of the satellite

- **Particle accelerators:** acceleration of particles will encounter protons and electrons, with high energy, which affect the control circuits.

2.3 Radiation effects on electronic circuits

Radiation has two major damaging scenarios for electronic devices and circuits as:

Lattice displacement: charged particles and very high-energy gamma photons causes lattice displacement where they change the arrangement of the crystal lattice increasing the number of recombination centers. On the other hand high doses of radiation over short time cause healing of the damaged lattice lowering the level of damage happened due to low doses over long time. This type of damage directly affecting transistors especially bipolar transistor as it depends on the minority carriers while this affects the transistor gain [14].

Ionization effects: charged particles with low energy generates photo current to flow creating some glitches and soft errors but it can lead to destruction of the device if they trigger other damage mechanisms as latch up [14].

2.4 Resultant effects of radiation

These damages can end up with higher level of damage can be considered as end user damages as:

- **Neutron effects:** based on the first basic damaging mechanism a highly charged particle such as neutron interacting with the lattice will displace its atoms. Recombination centers increase reducing the life time of the minority carriers which directly affects the bipolar transistors (more than CMOS devices). The electrical parameters of the bipolar transistor change at 10 Giga neutrons per square centimeters with respect to 1000 Tera in case of CMOS devices. This effect increases the sensitivity of the device with the level of integration [14].

- **Total ionizing dose effects (TID):** based on the lattice displacement damage cumulatively over long period. During the ionization process generation of electron hole pairs takes place in the gate oxide (insulation layer), while during recombination a photocurrent passes which is undesirable and can be considered leakage current and the holes trapped in the lattice defects as that insulator usually made from amorphous lattice. The prescribed mechanism biases the gate terminal and influences the threshold voltage of the transistor making the NMOS easier and the PMOS more difficult to switch on and this can turn to a permanent ON or OFF switching with time [14].

- **Transient dose effects:** short-time high-intensity radiation considered as a radiation pulse usually occurs during nuclear attacks and explosions. This high energy creates photocurrents in the semiconductor causing the transistors to randomly open changing the logical states of the memory elements such as flip-flops [14].

- **Single-event effects:** usually electronic circuits are affected with the single-event effects while the digital circuits are the most sensitive. Single-event happens due to the travelling of high-energy particle through a semiconductor leaving an ionized track behind it. This effect is similar to the transient dose effect forming a glitch at the output flipping the memory blocks [14].

2.5 Radiation hardened techniques

There are two types of radiation hardening, physical hardening and logical hardening and each of them has several techniques in order to eliminate or decrease the effects of the radiation on the electronic devices and systems.

- **Physical hardening:**

    - As previously mentioned that the major problem occurs due to either the travelling of a charged particle with high-energy in a semiconductor substrate or accumulation of energy affecting the generation and recombination rate in the semiconductor substrate. One of the techniques is manufacturing the hardened chips on insulating substrates instead of silicon wafers. Silicon on insulator (SOI) and silicon on sapphire (SOS) are commonly used in this aspect. This way allows the radiation-hardened chips fabricated on SOI or SOS to withstand many orders of magnitude of radiation those of silicon substrate [14].

    - Shielding the package of the integrated circuit against radioactivity can help in decreasing the exposure of the devices to radiation.

    - New devices are produced to be radiation hardened such as magneto resistive RAM replacing the other types of RAMs and providing rewritable, non-volatile conductor memory.

    - Wide band gap substrates such as: silicon carbide and gallium nitride can provide high tolerance to deep-level defects.

- **Logical hardening:**

    - Redundant elements and techniques usually used on the circuit level. "NMR" is one of these techniques where 3 images of every module are used and a separate "voting logic" to correct the fault happened as an effect of radiation. The disadvantages of this technique is that it increases the area of the design into 5 times also if the " voting logic" had a fault it will affect the result

    - Error detection and correction techniques such as parity bits to detect the errors occurred due to radiation faults and possibly correct them.

    - Some errors due to radiation faults change the state of the system if it is based on FSM sequential logic. System reset can be a good solution to this problem, which could be done using a watchdog timer. The watchdog timer performs a hard system reset unless it receives a certain sequence indicating the system is alive.

Chapter 3

CONCEPTUAL FRAMEWORK

3.1 Floating Gate MOSFET (FGMOS)

A floating gate transistor is a type of MOSFET transistor with a similar structure to the MOSFET except that the gate of the FGMOS, as shown in fig. 1, is electrically isolated , which creates a floating node in DC and another secondary gate deposited above it , where the inputs are capacitive connected to the FG.

The charge stored on the FG remains unchanged so it could be used as a memory like EPROM , EEPROM and flash memories because it keeps its state for long periods of time, and it could be used as a connecting switch, which is the case in FPGA Flash based connecting switches [1].

Fowler – Nordheim tunneling and hot- carrier injection mechanisms are used to modify the charge stored in the FG whether increasing or decreasing it.

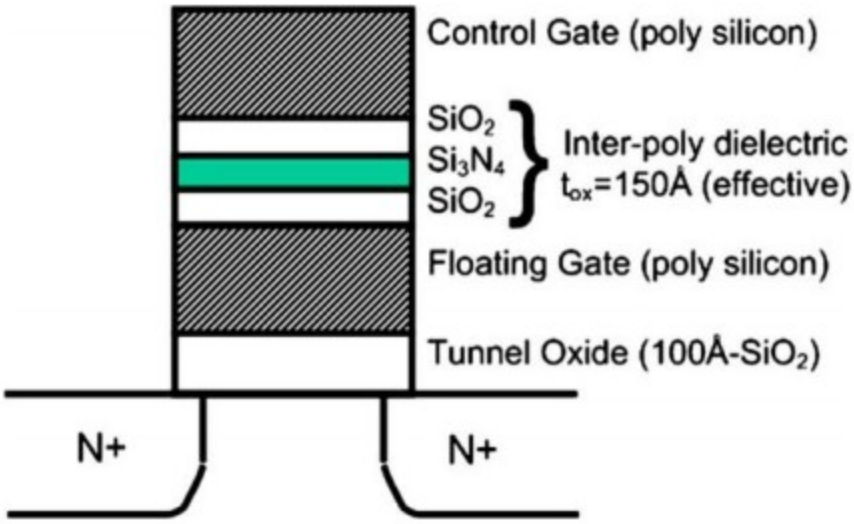

Figure 1 FGMOS [1]

3.1.1 FGMOS ON state

During the on state of the floating gate transistor, a high electric field between the drain and source will result in injection of charges in the floating gate changing the threshold voltage. Excess charges can also be erased from the floating gate. The operation of the FG transistor is similar to the operation of a normal MOS transistor except that the gate voltage is replaced by the floating gate voltage and the transistor's threshold voltage value varies with varying the amount of charges stored in the floating gate [2].

With a rough hand analysis, the long channel model for the transistor [13] is as follows:

In the triode region $v_{DS} \leq v_{GS} - V_t$ and $v_{GD} \square V_t$ where v_{GS} is the FG to source voltage and v_{GD} is the FG to drain source

$$i_D = K_n' \frac{W}{L} \left[(v_{GS} - V_t) V_{DS} - \frac{1}{2} {v_{DS}}^2 \right] \qquad (1)$$

if $v_{DS} << v_{GS} - V_t$

$$i_D = K_n' \frac{W}{L} [(v_{GS} - V_t)V_{DS}] \qquad (2)$$

$$i_D = K_n' \frac{W}{L} [(v_{GS} - V_t)^2] \qquad (3)$$

and the resistance of the transistor in the "ON" state will be

$$r_D = \frac{v_{DS}}{i_D} = \frac{1}{k_n' \frac{W}{L}(v_{GS} - V_t)} \qquad (4)$$

If the transistor has a high positive threshold voltage, there will be no channel and the transistor will be off.

If the transistor has a negative threshold voltage, then there will be a channel, the transistor will operate in the triode mode, and the channel resistance will be

$$r_D = \frac{1}{k_n' \frac{W}{L}(v_{gs}' + |V_t|)} \qquad (5)$$

This means that channel resistance is inversely proportional to the threshold voltage. With total dose decrease of the positive threshold voltage, this will result in an increase in the channel resistance.

3.1.2 FGMOS threshold voltage

The threshold voltage of the FGMOS is directly proportional to the amount of charges stored on the floating gate. The amount of charges can be changed either by Fowler – Nordheim tunneling or hot- carrier injection mechanisms.

Some recent researchers derived a closed form equation as appears in eq. (6) for the dependence of the FGMOS threshold voltage on the charges stored on the floating gate [2].

$$V_{th} = V_{si} + \frac{Q_{fg}(0)d_{ono}}{\varepsilon_{ox}}. \qquad (6)$$

3.1.3 Simulation of FGMOS ON mode

Simulation of FGMOS ON mode is like the simulation of any NMOS transistor except that the threshold voltage will be negative and high in value even when the gate voltage is zero. The resistivity of the channel will increase as the threshold voltage decreases in value (becomes less negative).

3.2 TID induced effects on FGMOS

TID induced effects on the FGMOS appear directly in the change in floating gate stored charges, which vary the threshold voltage value due to the direct dependence of the transistor threshold voltage on the floating gate stored charges as stated before in eq.(6) . The threshold voltage with TID is dependent on the state of the FGMOS whether it is the ON state or the OFF state. Different experiments previously investigated the threshold voltage variation with TID at the two states of the FGMOS where a significant decrease in the threshold voltage magnitude value $|V_{th}|$ appears with increasing the TID in both states as shown in fig. 2 [1] [2].

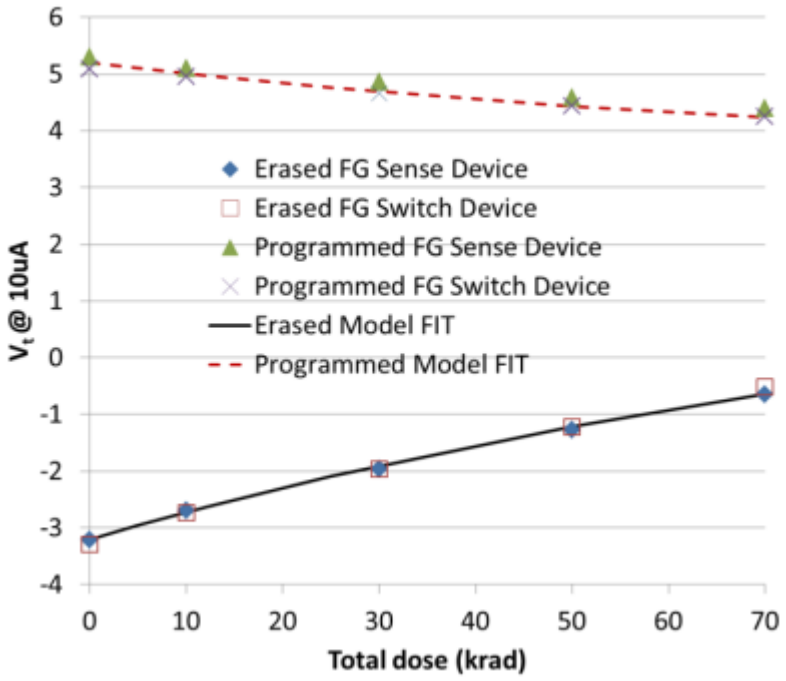

Figure 2 Threshold voltage variation across vs. TID increase at 65nm technology [1].

3.3 FGMOS threshold voltage variation effect

Degradation in the FGMOS threshold voltage on the device level affects the important electrical parameters on the circuits and systems level, such as propagation delay of the system and the amount of leakage current lost in the circuit, where these parameters could lead to propagation delay or/and leakage current failures[4][5].

The propagation delay and the power current at the device level were previously studied in [4] where they were characterized versus the TID in different situations. A significant increase in the propagation delay values were measured proportional to the increase in TID as shown in fig3.

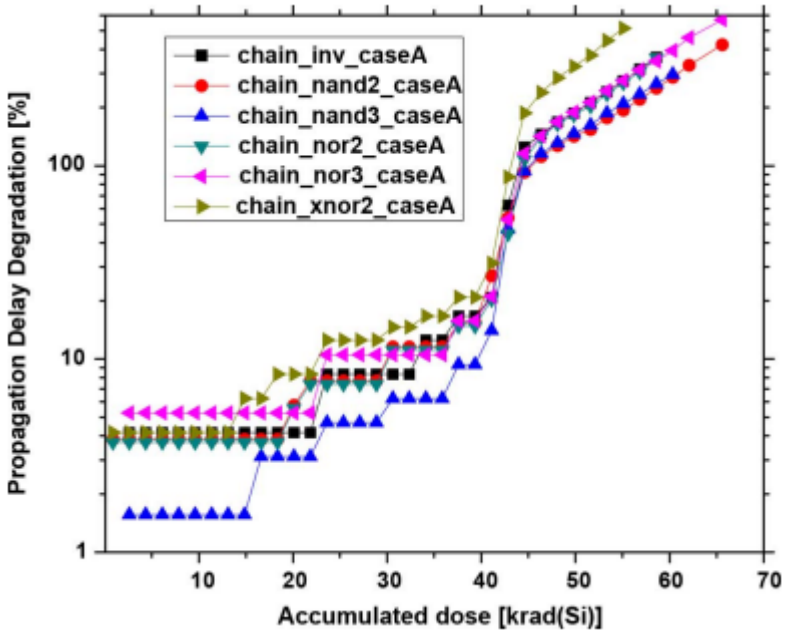

Figure 3 Propagation delay degradation vs. TID[4].

Chapter 4

FAULT MODELS AND WCTVS GENERATION

In this chapter a novel methodology for identifying the worst – case test vector for a combinational circuit of FPGA devices exposed to total dose will be introduced based on previously developed fault models for delay and leakage current failures for ASICs[15][16][17][18] .

4.1 Introduction

The total dose testing standard, MIL-STD-883[20], method 1019, emphasizes the use of worst – case test vectors WCTVs. However, they are typically not used in total-dose testing of FPGA devices because they are known to be almost impossible to be identified for most VLSI devices. A couple of methodologies were proposed to identify WCTVs for both propagation delay and leakage current failures induced by total ionizing dose (TID). The search space for WCTVs is 2^{2n} , where n is the number of primary inputs of the circuit under test .

In this work, A methodology is developed for the FPGA devices with a large number of gates even with a large number of inputs, which could be processed in a reasonable time: this was achieved by developing a searching algorithm based on the genetic algorithm. After some development, Mentor Graphics tool (Fast Scan) showed a great accuracy for identifying the test vectors for specified path during propagation delay failure test.

WCTVs can help in identifying the expected damage in the design exposed to radiation effects which is done offline after the designing process which can help in changing the layout of the design to keep the radiation critical paths away from the critical logical paths which makes the design more robust against radiation . Furthermore knowing the WCTVs can help during the operation of the design on the FPGA chip where after certain damage which happens during a previously calculated period according to the rate of the radiation, which is known for the surrounding environment of the FPGA chip. This help can be represented in avoiding certain inputs for the design so as not to be exposed to the propagation delay failure for those vectors.

4.2 Fault model

The fault model is an abstraction of a given failure at a certain level of circuit representation that is performed to simplify the process of generating test vectors.

4.2.1 Propagation delay failure

The problem of propagation delay failure is a two-fold problem: first, there is the versatile cell propagation delay and secondly, there is the propagation delay due to the floating gate switches connecting the versatiles together. We can classify them into

- Versatile propagation delay
- Inter-Versatile propagation delay

The versatile cell has some internal CMOS components the form of some inverters, nor gates and multiplexers while the floating gate (FG) transistors form the connection switches between these ingredients building a configurable logical design which can be configured to perform different logical operations in a similar way for that used in the look-up tables used in the other types of FPGAs.

Each versatile block has a certain delay depends on its type which can present the problem of the identification of the main reason for difference in the propagation delay for the different types of the logical cells. For every design, obviously there will be a long path between different inputs and different outputs, which introduce the need for the investigation of inter-versatile propagation delay, which helps in building a model valid to be used in several designs.

Both the folds of the problem express a need for the investigation of the relation between the propagation delay and the number of floating gate transistors to be used in building a propagation delay models for both the versatile propagation delay and inter-versatile propagation delay.

4.2.2 Leakage current failure

The problem of leakage current failure is a two-fold problem too: first, there is the MOSFET transistor leakage current and secondly, there is the floating gate transistor leakage current.

The MOS transistor builds the logical cells which represent the ingredients of the digital design while the floating gate (FG) transistors form the interconnections between the cells and nets. Furthermore, In Proasic 3 FPGA the floating gate transistor is used in the internal connections of the custom building block used to build all types of cells (versatile) and also used in the inter-versatile connections.

The conditions of leakage current in both MOS transistors and FG transistors depend on the variation in the threshold voltage, while the mechanism of the change in the threshold voltage in both cases is different.

Chapter 5

PROPAGATION DELAY FAILURE

This chapter investigates the delay failure induced in the FPGA cells by TID .

A novel cell-level fault model was developed to analyze the delay failure on the level of the separate cell based on the model of the programmable versatile unit, which is internally programmable with different internal switches configuration forming the various types of standard cells supported by the FPGA as well as different versions of each cell type according to the way of connecting the switches.

This fault model is was used to identify the WCTV for delay failures and is supported by SPICE simulations validated with TID experiments in a cobalt 60 radiating unit.

5.1 Introduction

Despite the emphasis in total – dose testing standard , MIL-STD-883[20], method 1019 , on using WCTVs, they are typically not used in total dose testing of FPGA devices as they are almost impossible to be identified. A methodology to identify the WCTVs for delay failures induced by TID for FPGA devices is developed . This methodology follows the typical design flow of FPGA devices and their supported cells. A smart searching algorithm using directed graph and genetic algorithm has been introduced for identifying WCTV for all FPGA devices [3].

5.2 Failure analysis

In this effort, Mircrosemi ProASIC3 FPGA, a flash-based, 130-nm LVCMOS process with seven layers of metal was used. The proprietary architectures of the ProASIC3 device provide granularity comparable to gate arrays. The device core consists of an array of Versatile architecture. Each Versatile can be configured to up to three-input logic cells or as a D-flip-flop (with or without enable), or as a latch as shown in **Error! Reference source not found.** by programming the appropriate flash switch interconnections.

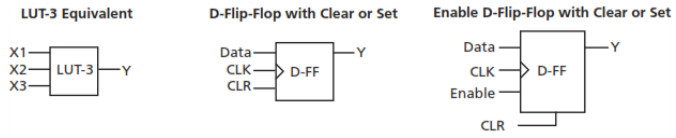

Figure 4 types of Versatile cell configurations[6].

The internal gate-level schematic diagram of the Versatile is shown **Error! Reference source not found.** [6]. As shown in the figure, it consists of 11 inverters, 1 2-input nor gate, 4 2x1 multiplexers, and 31 floating-gate switches. Versatile can flexibly map the logic and sequential gates of a design. The inputs of the Versatile can be inverted, and the output of the tile can be connected to high-speed, very-long-line routing resources. Versatile and larger functions can be connected with any of the four levels of routing hierarchy. The output of the Versatile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources.

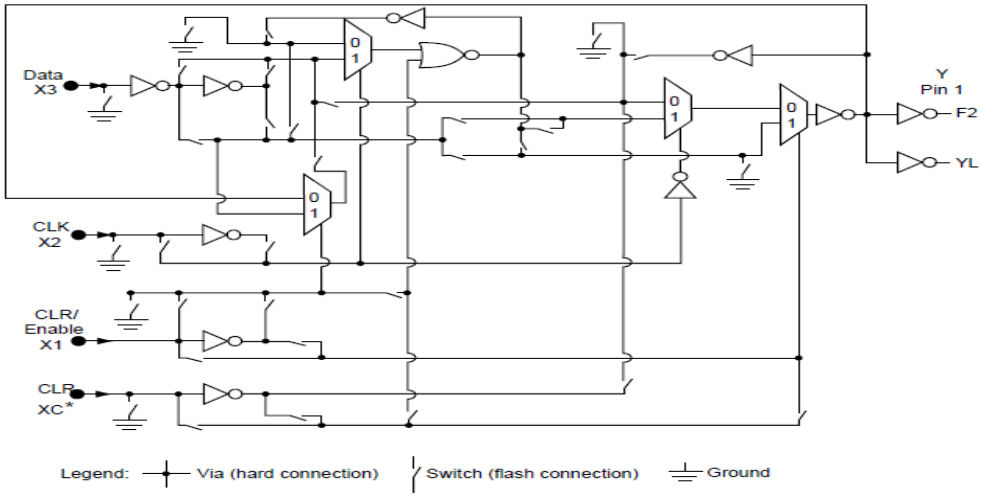

Figure 5 Gate-level schematic diagram of ProASIC3 Versatile[6].

ProASIC3 is a low power flash device, which uses a flash switch as its programming element. Flash cells are distributed throughout the device to provide nonvolatile reconfigurable programming to connect signal lines to the appropriate versatile inputs and outputs. In the flash switch, two transistors share the floating gate, which stores the programming information as shown in **Error! Reference source not found.**. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. The latter is used to connect or separate routing nets, or to configure versatile logic. It is also used to erase the floating gate.

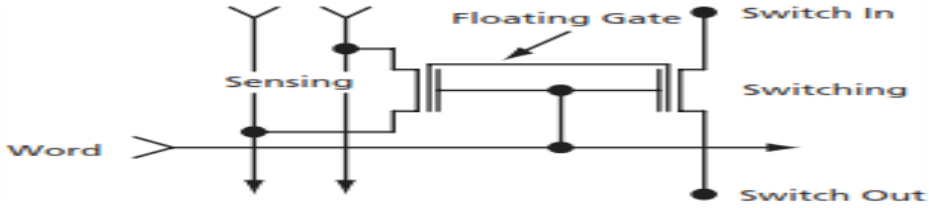

Figure 6 Schematic of the floating-gate switch[6].

The Versatile can be configured to give a rich library of combinational and sequential cells [7]. A few examples of those cells are shown in Table I.

TABLE I
EXAMPLES OF DIFFERENT VERSATILE CELL CONFIGURATIONS

Category	Cell
Basic Logic Gates	*AND2, AND2A, AND2B, AND3, AND3A, AND3B, AND3C, BUFF, BUFD, INV, INVD, MX2, MX2A, MX2B, MX2C, NAND2, NAND2A, NAND2B, NAND3, NAND3A, NAND3B, NAND3C, NOR2, NOR2A, NOR2B, NOR3, NOR3A, NOR3B, NOR3C, OR2, OR2A, OR2B, OR3, OR3A, OR3B, OR3C, XNOR2, XNOR3, XOR2, XOR3*
AND-OR	*AO1, AO12, AO13, AO14, AO15, AO16, AO17, AO18, AO1A, AO1B, AO1C, AO1D, AO1E, AOI1, AOI1A, AOI1B, AOI1C, AOI1D, AOI5*
OR-AND	*OA1, OA1A, OA1B, OA1C, OAI1*
Sequential	*DFN1, DFI1, DFN1C1, DFN0C1, DFN1E1C1, DFN0E1C1, DLN0P1C1, DLI0P1C1*
Input/ Output	*BIBUF, CLKBIBUF, CLKBUF, INBUF, OUTBUF, TRIBUFF*
Others	*AX1, AX1A, AX1B, AX1C, AX1D, AX1E, AXO1, AXO2, AXO3, AXO5, AXO6, AXO7, AXOI1, AXOI2, AXOI3, AXOI4, AXOI5, AXOI7, MAJ3, MAJ3X, MAJ3XI, MIN3, MIN3X, MIN3XI, XA1, XA1A, XA1B, XA1C, XAI1, XAI1A, XO1, XO1A*

Previously, total-ionizing-dose effects on Mircrosemi the Pro-ASIC Plus flash-based FPGA were systematically investigated [8]. Proasic Plus is a 220 nm and 4 metal layer technology. At moderate total dose range of 10 to 20 Krad, the radiation response of the Pro-ASIC plus FPGA is dominated by the threshold voltage shift of the floating gate device. The propagation delay data are measured on a 1000-stage inverter string. The actual physical circuit has "programmed" switches linking these inverters. The experimental data shows that in unbiased radiation, the average degradation is 3.6% after 20 Krad and for biased radiation; the average degradation is 6.3% after 20 Krad. Another effort was carried out to experimentally characterize the radiation effects of Mircrosemi the Pro-ASIC [9]. Again a chain of 1000 inverters was used and clocked at 1 MHz The device functional failure due to delay degradation was exhibited at a total dose of 65 Krad.

Different factors contributing to delay failure induced by total dose in an attempt to identify the worst-case conditions for delay failure were explored. The schematic diagram of the Versatile

shown in **Error! Reference source not found.** indicates that there are 31 floating-gate switches used to configure the Versatile into the different cells. Unfortunately, the mapping of the settings of those 31 switches to the different cells within the cell library is proprietary. However, Being able to estimate the setting of those switches for each cell using the logic function of each cell. Consider for example a Versatile configured as an OA1A cell as shown in **Error! Reference source not found.**. the best guess is that the internal switches inside the versatile are set as shown in **Error! Reference source not found.** which indicates that there are 2 switches along the path from the A input to the Y output and 1 switch along the path from B to Y and 1 switch from C to Y.

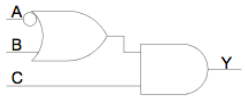

Figure 7 Versatile configured as OA1A cell.

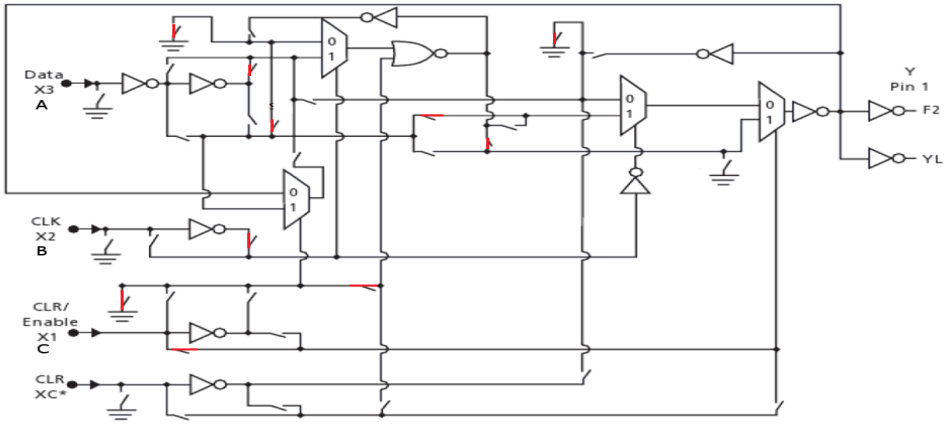

Figure 8 Switch setting of Versatile configured as OA1A cell.

We also analyze BUFF cell shown in Fig.9. The switch setting for this cell is shown in **Error! Reference source not found.**. It indicates that along the path from A input to Y output there is only one floating gate switch.

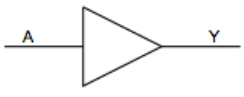

Figure 9 Versatile configured as BUFF cell.

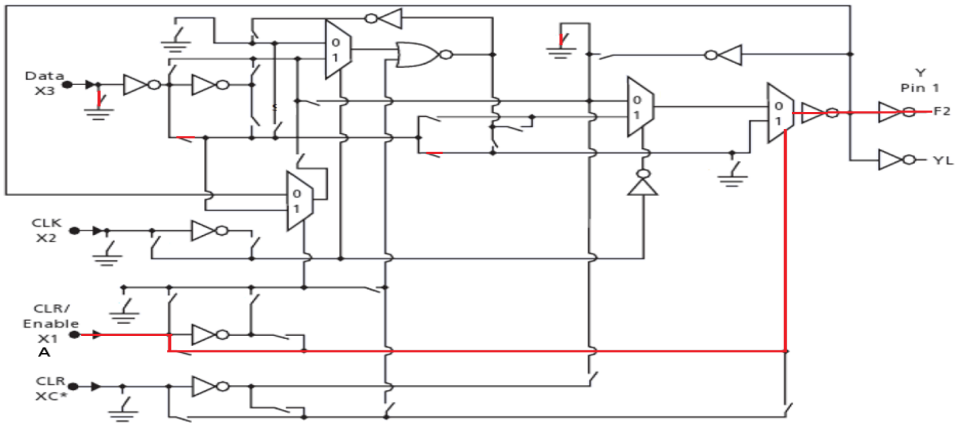

Figure 10 Switch setting of Versatile configured as BUFF cell.

The analysis of the different cells within the versatile library indicates that along the path from the inputs to the outputs of most of the combinational logic cells, there might be either one or two switches along the path from the inputs to the output. The important conclusion from this analysis is that cells with two switches will exhibit higher delay failure than those with single switch. In addition, within the same cell different inputs may have different delay failure depending on the number of the switches along the path from input to output.

5.2 Fault model of delay failure induced by TID

Fault modeling is a technique for abstracting a given failure mechanism at a certain level of circuit representation for generating test vectors [10]. In this section, A novel fault model that represents the delay failure induced by total dose at the cell level of the FPGA is presented.

If we have a chain of n cells of the same type, then the delay along the chain, t_{pd}, will be equal to

$$t_{pd} = n \times t_d + m \times t_{net} \qquad (7)$$

where, n is the number of cells within the chain, t_d is the propagation delay of the cell, m is the number of routing nets within the chain, and t_{net} is the average delay of the routing nets. It should be noted that every cell in the chain has an input net and output net and every net has at least one floating gate switch. Therefore, $m \geq n + 1$, and consequently m is somehow related to n.

The cell propagation delay t_d and the net delay t_{net} can be described as follows:

$$t_d = \hat{t}_d + k \times t_{sw}, \quad (8)$$
$$t_{net} = \hat{t}_{net} + t_{sw} \quad (9)$$

where, t_{sw} is the delay of the floating gate switch, k is the number of floating gate switches inside the Versatile along the path from the input to the output of the cell, $\hat{t}_{pd}$ and $\hat{t}_{net}$ are propagation delay and net delay without the switch delay.
As the total dose increases, the switch delay also increases $\bar{t}_{sw} = t_{sw} + \Delta t_{sw}$ while the delay of the logic gates with the cells can be neglected [8][9]. Consequently, the delay along the chain will be

$$\bar{t}_{pd} = t_{pd} + \Delta t_{sw}(k \cdot n + m) \quad (10)$$

where, $\bar{t}_{pd}$ is the propagation delay of the chain because of total dose and Δt_{sw} is the increase of the delay of the floating gate switch because of total dose. Therefore, the increase of chain delay because of total dose will be

$$\Delta t_{pd} = \bar{t}_{pd} - t_{pd} = \Delta t_{sw}(k \cdot n + m) \quad (11)$$

This equation models the increase of propagation delay with the increase of number of switches due to the total dose.
We need to experimentally validate the above fault model. We used Mircrosemi ProASIC3 A3P125-208PQFP FPGAs and configured them with chains of cells. Each chain has an *n* number of cells of the same type. We have different chains with different cells. The FPGAs were then exposed to Cobalt 60 at dose rate of 100 rad/sec. We then measured the increase in propagation delay of those chains. Fig.11 shows the relationship between the increase in propagation delay of chains of OA1A cells with different number of cells per chain and at different total dose levels. This figure confirms the delay model expressed in equation (11) and that the increase in propagation delay because of total dose is linearly proportional to the number of cells within the chain. Fig 11 shows the increase of delay in two chains: one with OA1A cells ($k = 2$) and another with BUF cells ($k = 1$). This also indicates that cells with ($k = 2$) exhibit higher delay increase than chains with cells with ($k = 1$).

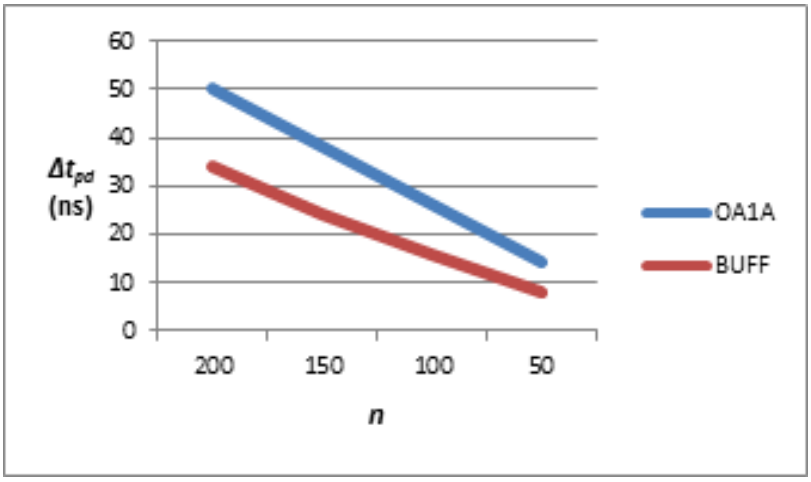

Figure 11 Comparing delay in chains of OA1A and BUFF cells at 60 Krad.

5.2 Worst – case delay conditions

Contemporary FPGA design guidelines emphasize the use of synchronous circuits where the design is divided into domains and each domain is synchronized by a different clock. The maximum operating frequency for a given synchronous circuit is determined using a model of combinational circuit in between an input register and an output register as shown in **Error! Reference source not found.**

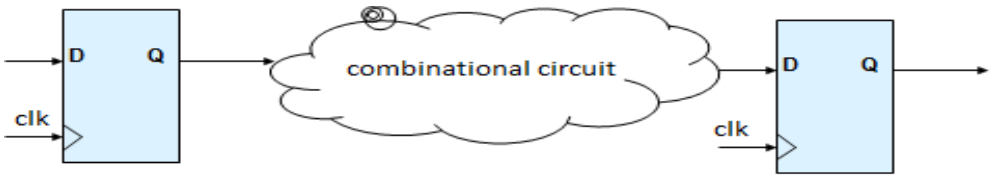

Figure 12 Model for synchronous circuit.

The clock frequency f_c is determined by the system specifications. The clock period, $T_c = 1/f_c$ and must satisfy the following inequality [12]

$$T_c \geq t_{pd} + t_{cq} + t_{su} \quad (12)$$

where t_{pd} is the propagation delay of the combinational circuit between the two registers, t_{cq} is the clock-to-output time of the input register, and t_{su} is the required setup time for the output registers. Both t_{cq} and t_{su} depend on the characteristics of the flip-flops for a given cell library and they are not circuit dependent. A setup slack is depicted in **Error! Reference source not found.** and is defined as the difference between required arrival time of the edge of the data and the actual arrival time of the edge of the data which can be express as [12]

$$Slack_{su} = T_c - (t_{pd} + t_{cq} + t_{su}) \tag{13}$$

A positive setup slack will result in proper functional operation of the system. However, a negative slack will result in a functional failure due to the violation of the required setup time. FPGA exposed to total dose will result in increase in t_{pd} and consequently decrease of the setup slack.

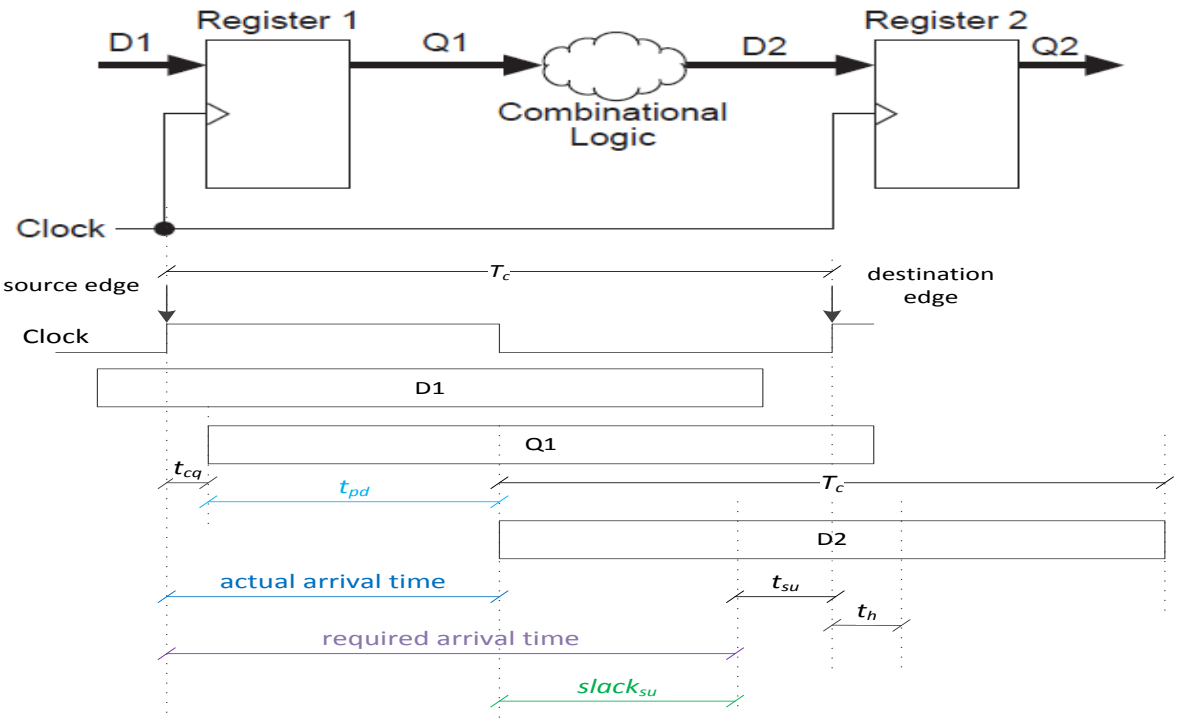

Figure 13 Model for setup slack.

Different paths within the design will result in different propagation delays. A critical path is the one that will result in the longest delay. The worst-case condition of the delay failure due to total ionizing dose will correspond to the worst-case path that is the one that will result in a maximum increase in delay. The worst-case path will then be the one that corresponds to the path with the maximum number of floating gate switches

$$\{\Delta t_{pd}\}_{worst-case} = \Delta t_{sw} \cdot max\{(k \cdot n + m)\} \quad (14)$$

Although equation (14) is simple and straight forward, the search space for worst-case test vectors for delay failure is rather huge even for small circuits. This is not just because of the number of possible combinations at the primary inputs but because we also need to search for all paths between every two registers. This novel methodology that uses a mixed approach between static timing analysis (STA) and search techniques for worst-case test vectors. Static timing analysis is a method of validating the timing performance of a design against certain timing criteria such as maximum clock speed. The STA tool breaks down the design into sets of timing paths by checking all possible paths. It then calculates the signal propagation delay along each path and checks for violations of timing constraints inside the design and at the input/output interface. We then search for the correct input vector for a given path. Then we search for the longest path from the input to the output that maximizes the number of switches taking into consideration that there should be no masking for the toggled signal along this path.

We developed a novel technique for identifying worst-case test vectors, which can be described as follows:

1. Use the static timing analysis (STA) tools to identify a number of critical paths for a given design.
2. Identify worst-case paths by choosing critical paths with maximum number of floating gate switches.
3. Toggle the worst-case path with an input data alternating between 1 and 0.
4. We then search for logic values at the primary inputs that grantees the toggling of data at the starting point of the worst-case path all the way to the end of the path. In other words, we search for logic values at the primary inputs that avoid masking the toggling of the data along the worst-case path.

Chapter 6

EXPERIMENTAL WORK

This chapter will focus on validating the fault model on different levels (Cell level, Design level) using different types of illustrative designs then a total dose radiation was applied on these designs to validate the fault model to be used in the WCTV identification.

6.1 Introduction

A novel cell-level fault model was developed to analyze the delay failure on the level of the separate cell based on the model of the programmable versatile unit, which is internally programmable with different internal switches configuration forming the various types of standard cells supported by the FPGA as well as different versions of each cell type according to the way of connecting the switches .

6.2 Methodology

Using very clear steps, a fault model for the different cells was created to be used in building a larger design fault model where these steps were as follows:

1. Assuming some points to build the cell level fault mode
2. Doing some illustrative designs to be used to prove the assumptions
3. Applying total dose radiation experiments on the illustrative designs for the cell model
4. Checking the true and false assumptions
5. Building the cell level fault model
6. Making new assumptions to build the design level fault model

7. Doing illustrative designs to be used to prove the assumptions

8. Applying total dose radiation experiments on the illustrative designs for the design model

9. Checking the true and false assumptions for the design level model

10. Building the design level fault model

This fault model is used to identify the WCTV for delay failures and is supported by SPICE simulations validated with TID experiments in a cobalt 60 facility.

6.3 Cell & design level fault models

Building a cell level a fault model needed some assumptions to be proved in later stages while the first assumption was that the propagation delay is proportional to the number of cells and proportional to the total dose while this assumption is validated with a radiation experiment .

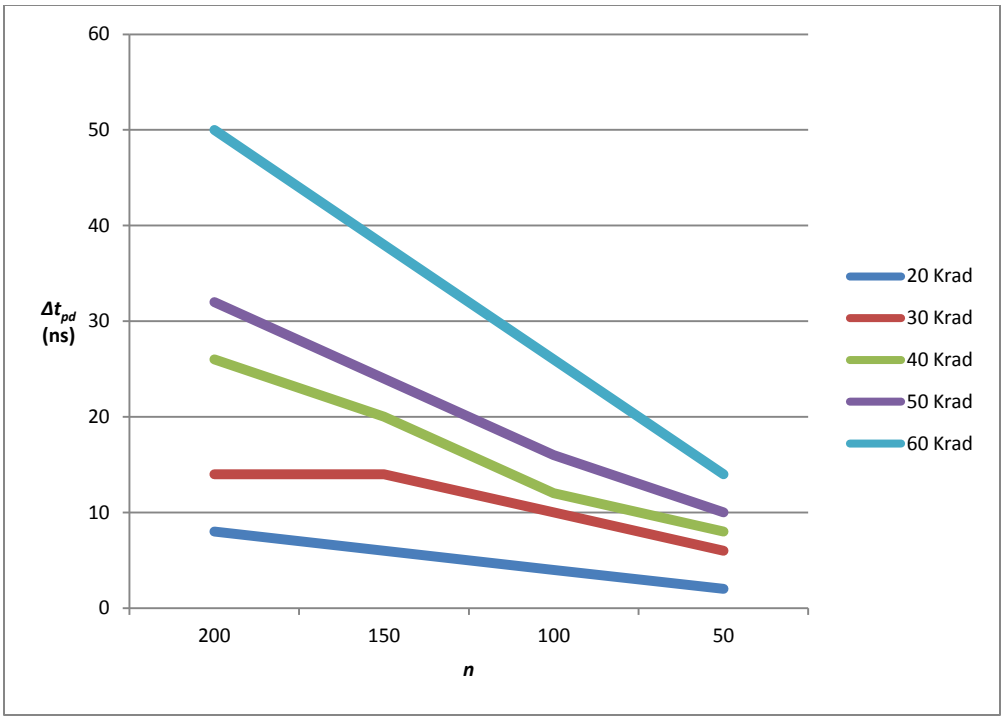

Figure 14: Delay variation versus number of switches for chain of inverters at differnt doses

In fig 14 it is clear that the propagation delay is increasing with the number of switches while it is proved that with increasing the total dose. According to this experiment, the assumption of the dependency of the propagation delay on the number of cells and the total dose is validated.

After studying the propagation delay for different types of cells, to discover the variation of propagation delay with the total dose for different types of cells. The results shown in the graph of figure 14 express the clear fact that the propagation delay varies with cell type while in all the cells it increases with the total dose, this investigates a new issue by classifying the delay of the cells according to their type .

So now the last step needed to build the cell level fault model is to study the main difference between the different types of cells and the effect of the space radiation on it.

An assumption was made claiming that the main point of difference between the cells is the number of switches inside the cell, which differs between a type and another; it also differs between two configurations of the same cell.

A new experiment to investigate both the effect of the number of switches, also the variation of the configuration can be investigated as it sounds as a variation in the number of switches. The experiment starts by generating all the combinations, which used to get different types of cells then identifying which cells that has combinations constant number of switches and the cells of combinations with variable number of switches, a python code used to do this. Two types of cells picked up for the experiment which are (NOR3-OR3) where the OR cell is the type that has constant number of switches for all the combinations while the NOR cell is the type that has variant number of switches with the different combinations.

During this experiment in building the cell fault model, 2 types of cells are used in 2 chains which can be routed successively in a way that they are routed next to each other as in Fig.15 so the dominant switches are the internal versatile switches. The same experiment can be used to build the design fault model so another 2 chains of the same cells are routed separately in a way that the dominant switches are the inter versatile routing switches as shown in Fig.15.

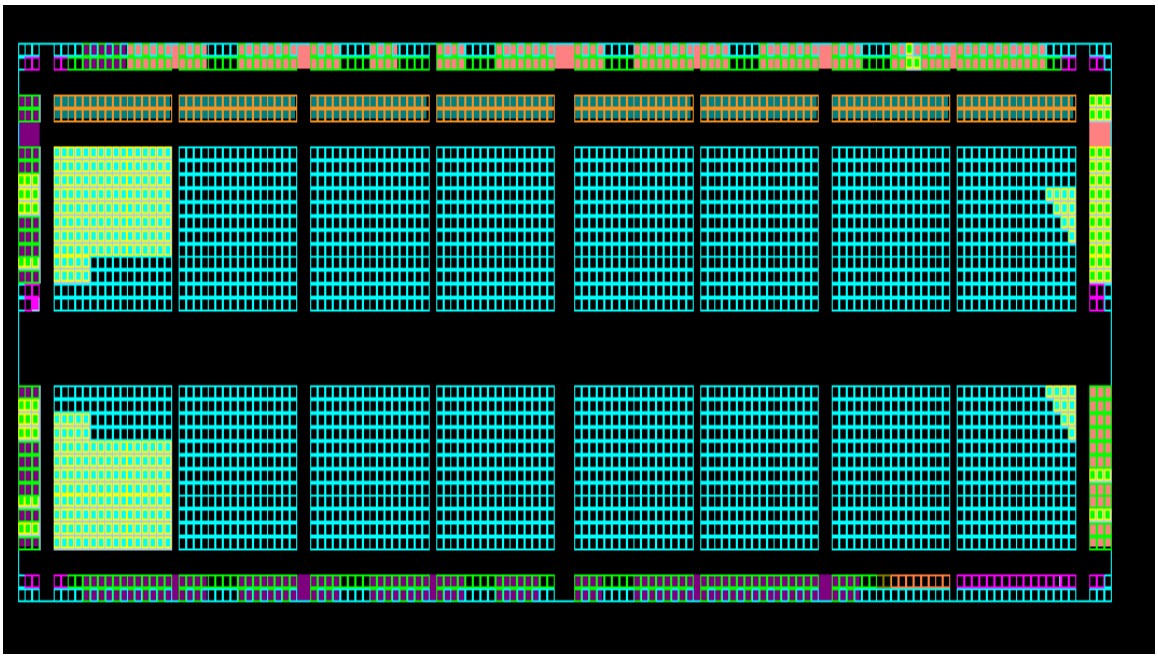

Figure 15: Layout of the OR & NOR cells

Chapter 7

EXPERIMENTAL RESULTS

7.1 Cell level fault model results

In a way of emulating the effect of the space radiation, a cobalt-60 radiating unit is used with a calculated radiation rate. With monitoring the propagation delay for different number of cells at specific total dose radiation values an insight about the relation between propagation delay and the total dose radiation amount with a high certainty about the main factor of the variation between a cell and another which can be used in building the cell level fault model.

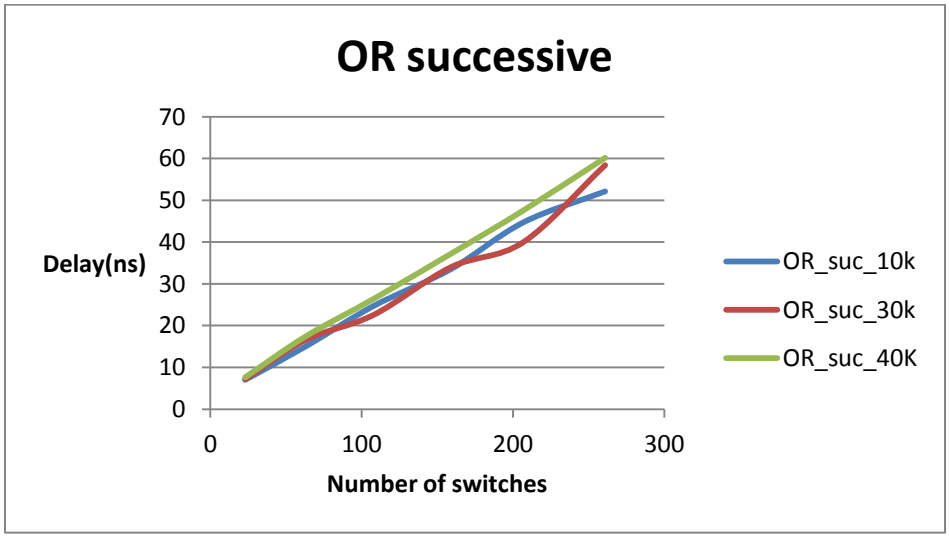

Figure 16: Propagation delay of succesive layouted OR chain

By analyzing Fig.16 it shows a relation between the propagation delay and the number of switches in the OR chain which had a constant number of switches for all the versatile switches combinations. The routing of the cells is based on a successive distribution so the dominant number of switches is the internal versatile switches. According to these conditions, the only included factor in this case is the number of internal versatile switches. It's very clear from the

graph that the propagation delay is approximately has a linear relation with the number of switches, while the family of curves show that for any switch count the propagation delay increases with increasing the total dose radiation amount.

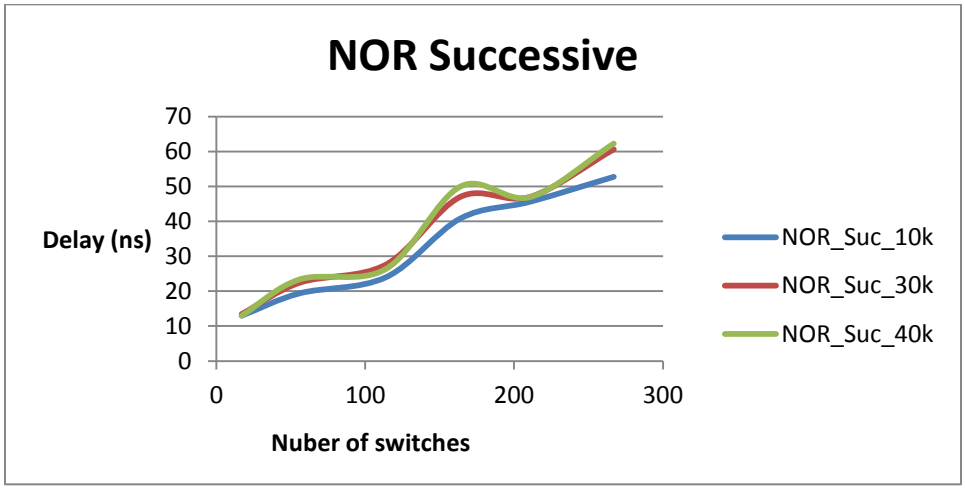

Figure 17: Propagation delay of succesive layouted NOR chain

Moving to another point by analyzing Fig.17 where another factor is included in the problem which is the switches configuration variation for the NOR cell. The routing of this chain is based on a successive routing similar to the previous case of the OR cells. This graph shows relation between the propagation delay and the number of switches (internal versatile switches) which tends to be linear while there are some variations showing the effect of the different switches configuration. Gain the propagation delay increase too with the amount of total dose radiation as in the previous case.

According to the previous analysis of this part of the delay chains experiment results a cell level fault model could be created easily based on the linear relation between the propagation delay and the internal versatile switches count, taking into consideration the different switches configurations for every cell to be included in the fault model.

7.2 Design level fault model

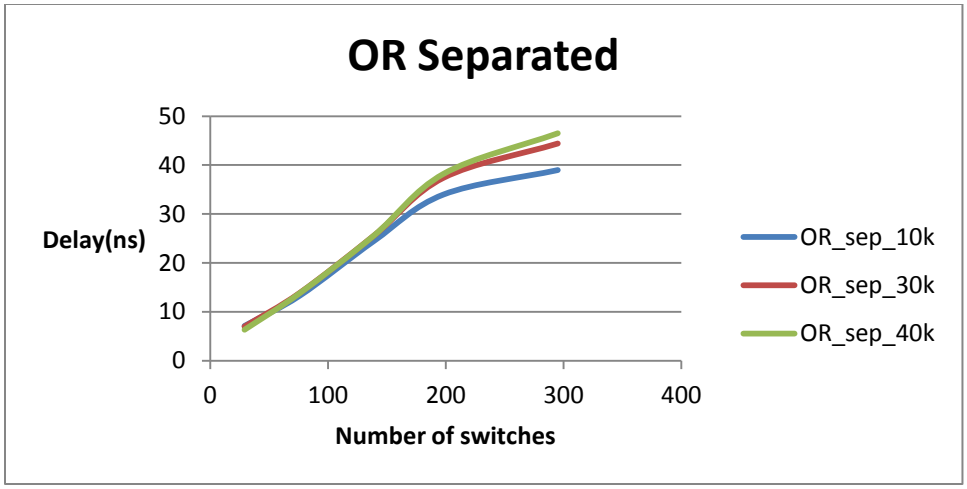

Figure 18: Propagation delay of separated layouted OR chain

In figure 18, a new factor is included in the discussed problem, which is the inter-versatile connecting switches count. This factor can help in creating the design level fault model, which can be built by the use the cell level fault model in addition to the analysis of the relation between the propagation delay of the chain and the inter-versatile connecting switches count.

The situation proposed figure 18 is very different from the previous ones, where the cells are routed separately in a way that makes the inter-versatile connecting switches are the most dominant switches. Similar as the previous cases by looking at the figure we can see that for the OR cells (with constant configurations) there is approximately a linear relation between the propagation delay and the number of switches but at this time it's the number of the inter-versatile switches which are the dominant switches.

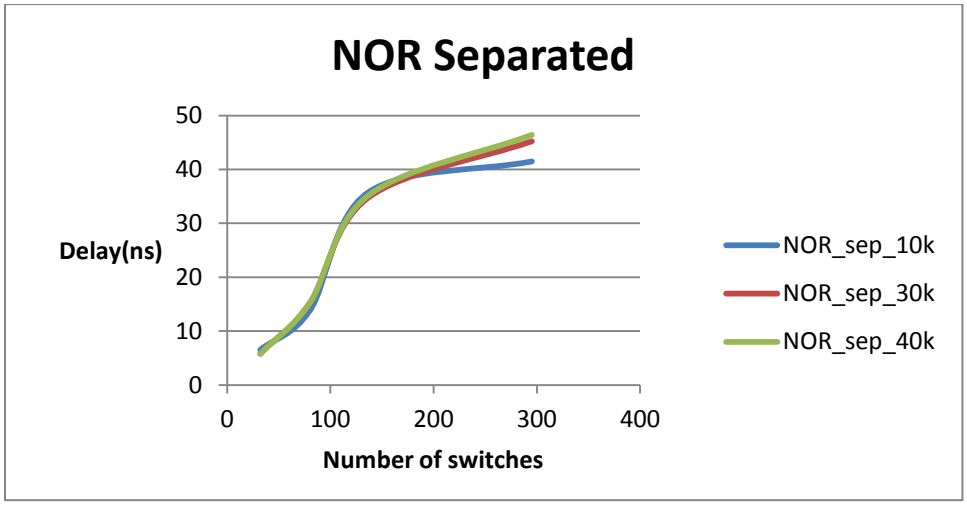

Figure 19: Propagation delay of separated layout NOR chain

The last figure adds another factor to the problem, which is using cells with variant, switches configuration and routed apart from each other to let the chance for the inter-versatile switches to be the dominant switches. The graph shows that the relation a bit changed due to the effect of the variation in the switches configuration.

Chapter 8

APPLICATION ON DESIGN

8.1 Multiplier Example

Consider for example the case of a multiplier design with two input operands, A and B, each of 8 bits while the output Product is 16 bits. Both the inputs and the outputs are registered. The multiplier was synthesized, placed and routed, using Mircrosemi Libero tools [7]. Table II summarized that different types of cells used to implement this multiplier along with number of floating gate switches in each cell and the corresponding number of instances the cell was used within the design. The STA tool indicates three critical paths. The one with maximum number of floating gate switches (a total of 43 switches) goes from A[3] to Product[12] as shown in **Error! Reference source not found.**. We searched for the test vector that will ensure the propagation of the toggling at A[3] will be manifested at Product[12]. It turns out that this vector be A=1010⇳101 and B=10101000 where, the symobol ⇳ denotes a toggling input between 0 and 1.

TABLE II
CELLS USED IN SYNTHESIZING 8X8 MULTIPLIER

Cell	Switches	Count	Cell	Switches	Count
AO1	2	25	DFN1E1C1	2	16
AO13	2	8	INBUF	1	18
AO1B	2	2	MAJ3	2	15
AOI1B	2	3	MX2	2	28
AX1	2	2	NOR2A	2	5
AX1B	2	1	NOR2B	3	38
AX1C	2	4	NOR3B	3	2
AX1D	2	8	NOR3C	2	11
AX1E	2	1	OA1	2	3
AXOI5	2	7	OA1A	2	3
BUFF	1	1	OR2	2	10
CLKBUF	1	1	OR2A	4	1
DFN1C1	2	17	XA1A	2	1
OUTBUF	1	17	XO1	2	1
XA1	2	28	XO1A	2	1
XA1A	2	1	XOR2	2	35
XNOR2	2	2	ZOR3I	2	3
XNOR3	3	2	**Total**		341
XOR3	2	21			

8.2 Multiplier example results

In this section, we want to experimentally assess the impact of using worst-case test vectors on the total dose level at which the design will cease to operate properly because of total dose induced delay failure in the FPGA. We again consider the case of the 8x8 multiplier discussed in Section IV. We assign a target timing constraint for the tools to implement the design on ProASIC3 A3P125-208PQFP so that it runs at a target frequency of 65 MHz or a clock period of $T_c = 15.4\ ns$. The multiplier was synthesized, placed and routed, using Mircrosemi Libero tools and the above timing constraint. The STA tool indicates three critical paths. The one with maximum number of floating gate switches (a total of 43 switches) goes from A[3] to Product[12] as shown in **Error! Reference source not found.**. The pre-rad propagation delay along this path $t_{pd} = 14.7\ ns$. Using Equation (13), a positive slack of $Slack_{su} = 15.4 - 14.7 = 0.7\ ns$ will result from using the worst-case test vectors A=1010⇳101 and B=10101000. Exposing the FPGA to total ionizing dose under this condition results in an increase of the propagation delay and a decrease in the slack. A delay failure will happen when slack becomes 0 ns or less. In this condition, total dose level at which there is delay failure is 20 Krad. We also searched for test vectors that correspond to two other cases: nominal and best cases. The corresponding slacks for all three cases are shown in **Error! Not a valid bookmark self-reference.**.

A comparison between total dose failure levels in all three test cases (worst, nominal, and best) is shown in

Table IV. The table indicates a significant difference in total dose failure levels between worst and nominal cases. Our experiments show all devices exhibit logic failure after 65 Krad.

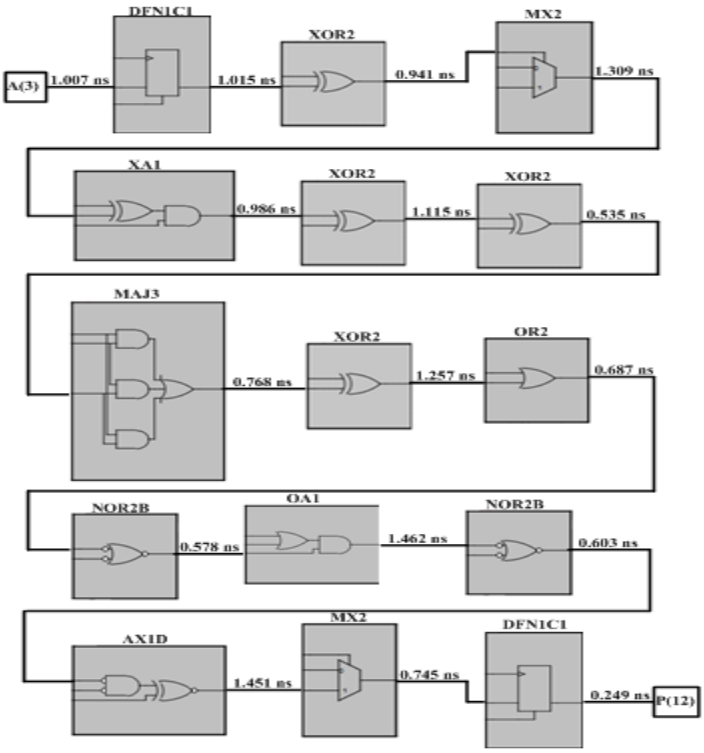

Fig 20: Worst-case path for the 8x8 multiplier

TABLE III
COMPARISON OF SLACK FOR THREE DIFFERENT CASES

Test Case	Start	End	n	t_{pd} (ns)	$Slack_{su}$ (ns)
Worst-case	A[3]	Product[12]	43	14.7	0.7
Nominal-case	A[2]	Product[4]	21	11.2	4
Best-case	A[1]	Product[1]	7	6.2	9.5

TABLE IV
COMPARISON OF TOTAL DOSE FAILURE LEVEL FOR THREE DIFFERENT CASES

Test Case	A	B	Failure Level (Krad)
Worst-case	1010⇳101	10101000	20
Nominal-case	00010⇳11	00001001	60
Best-case	110101⇳0	00011011	> 65

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Chapter 9

LEAKAGE CURRENT FAILURE

Floating gate transistor is the fastest element affected by ionizing radiation while this usually happens during the normal operation of the FPGA where the floating gate transistor acts as a switch in either ON or OFF steady state. Dealing with the floating gate switch in steady state can be similar to dealing with MOSFET transistor based on this the same drain current equations could be used in the investigation of leakage current in FPGA.

9.1 Leakage current failure

The leakage current for floating gate transistor is same as that of MOSFET transistor and corresponds to the drain current Ids during the cutoff or sub-threshold region.

$$I_{ds} = I_o * \frac{W}{L} * \left[1 - \exp\left(-\frac{V_{ds}}{v_t}\right)\right] * \exp\left(\frac{v_{gs} - V_{th} - V_{off}}{n * v_t}\right)$$

Where V_{th} is the threshold voltage, I_o and V_{off} are constants, v_t is the thermal voltage and n is the sub-threshold swing parameter. It is very clear that the drain current is inversely proportional with the threshold voltage variation with is the main effect of the ionizing radiation energy on the floating gate transistors. The leakage current induced by total ionization dose can be several orders of magnitude higher than the normal leakage current induced the transistor.

9.2 Fault model objective

leakage current sue to total ionization dose depends on dose amount, process technology, circuit design and the combination of irradiation and post-irradiation input vectors applied at the primary input of the circuit under test. The objective of the fault model is to have a methodology of measuring the leakage current at any dose level for all the input combinations. This fault model can be used in order to get the worst-case test vectors and they could be automatically generated using a tool to be built based on that proposed methodology.

9.3 Fault model basics

The leakage current failure occurred due to the floating gate transistors can be different from that CMOS circuit, as the leaking mechanism will usually happen when a switch is in the OFF state and one of its terminals is connected to the ground while the other terminal is connected to logic "1". Whenever this case happens, it will pass a current which isn't supposed to pass. This effect will be very clear as in Fig.21 at the switches connected to the input ports of the gate.

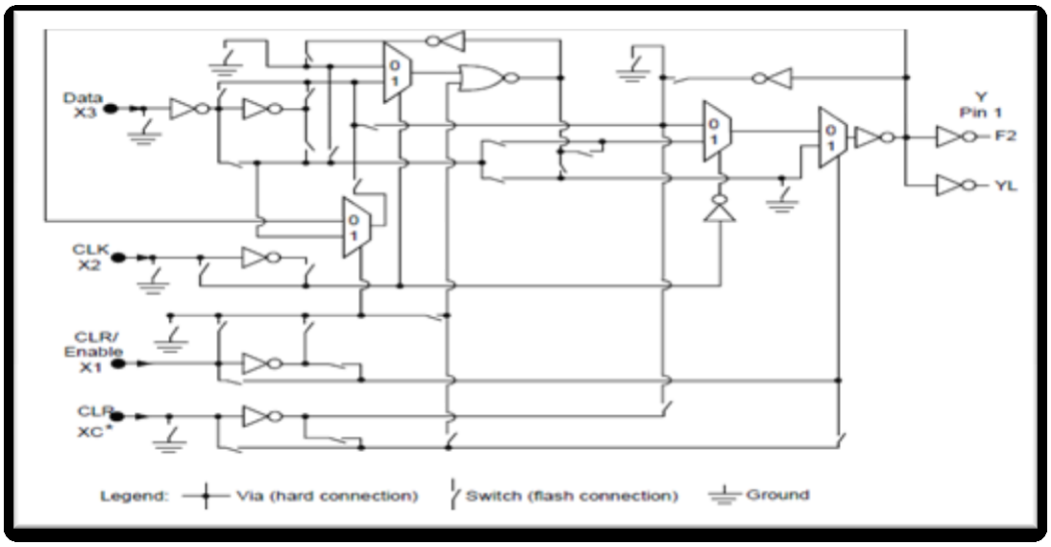

Fig 21: versatile schematic

According to the aforementioned mechanism, the leakage current needs to be measured at the input ports of the cell. Consequently, the total leakage current of the cell can be calculated as

$$I_{cell} = \sum_{k=0}^{n} (\mathrm{I_L})_K$$

Where n is the number of inputs, $\mathrm{I_L}$ is the leakage current measured at every input and k is the order of input port of the gate.

9.4 Fault model creation

The model creation is based on two main steps:

i. Simulation of the radiation effect on leakage current

ii. Experimental validation of the fault model by leakage current measurement

A spice model was built to simulate the effect of radiation on the leakage current. In this spice model a schematic diagram was built for the versatile cell where every gate was represented by its CMOS circuit and kept inside a symbol to be used as a black box like what is represented in the versatile while this schematic representation is shown in figure 22.

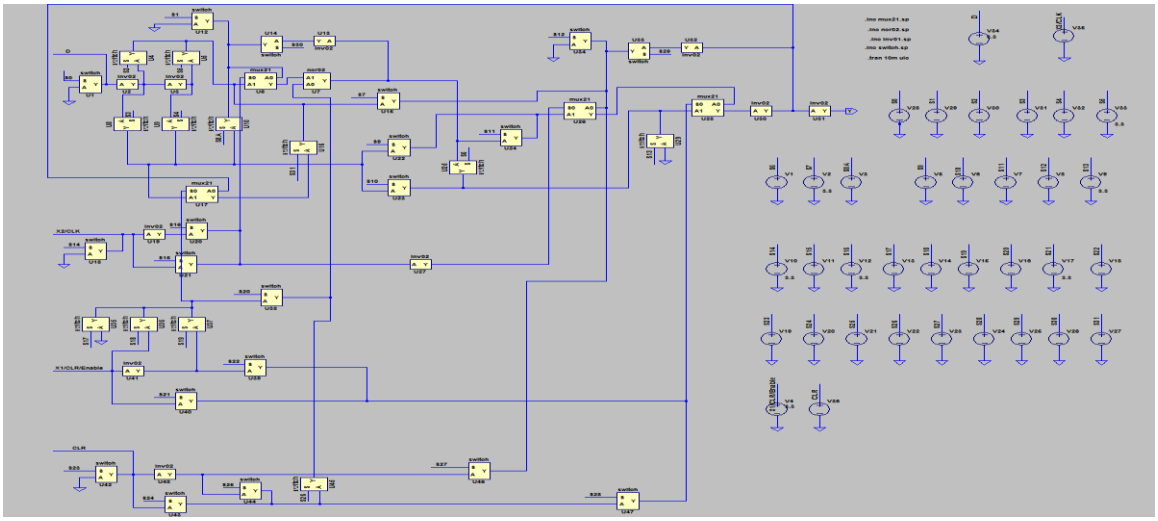

Fig 22: Versatile spice schematic

A schematic the floating gate switches are represented by n-type MOSFET where its threshold voltage is variable. A parametric sweep for the threshold voltage of all the floating gate transistor emulates the effect of radiation on this gate.

By adjusting the switches combination to form a OR3 gate a simulation for the leakage current value before and after the irradiation process while the results of this simulation in table proves what was previously postulated .

	Input 1		Input 2		Input 3	
Input combinations	Pre-Irradiation	post-Irradiation	Pre-Irradiation	post-Irradiation	Pre-Irradiation	post-Irradiation
000	0	0	0	-4.508E-05	0	-5.90E-05
001	1.21E-12	4.83E-05	0	-4.508E-05	0	1.21E-12
010	0	6.16E-31	2.42E-12	6.72E-05	0	-1.04E-04
011	0	0	1.10E-04	0.00E+00	-5.93E-05	2.42E-12
100	1.21E-12	4.83E-05	0	-4.51E-05	0	4.28E-05
101	1.21E-12	4.83E-05	0	-4.51E-05	2.42E-12	4.28E-05
110	1.21E-12	4.83E-05	2.42E-12	6.72E-05	0	-5.93E-05
111	1.21E-12	4.83E-05	2.42E-12	6.72E-05	2.42E-12	4.30E-05

9.5 Fault model validation

Simulation results usually are not efficient to build fault models but these results could be a guideline for experimental validation for the proposed fault model. An experiment to validate the fault model was done where it was based on creating a column matrix of OR3 cells as shown in figure 23 sharing the same input pins while the output of every group of cells terminates at a different pin and the count of these cells is very large so as to fill approximately all the FPGA chip . The idea of having so many cells as shown in the layout in figure 24 is to maximize the leakage current derived from the input pins to be large enough to be measured using the available instruments.

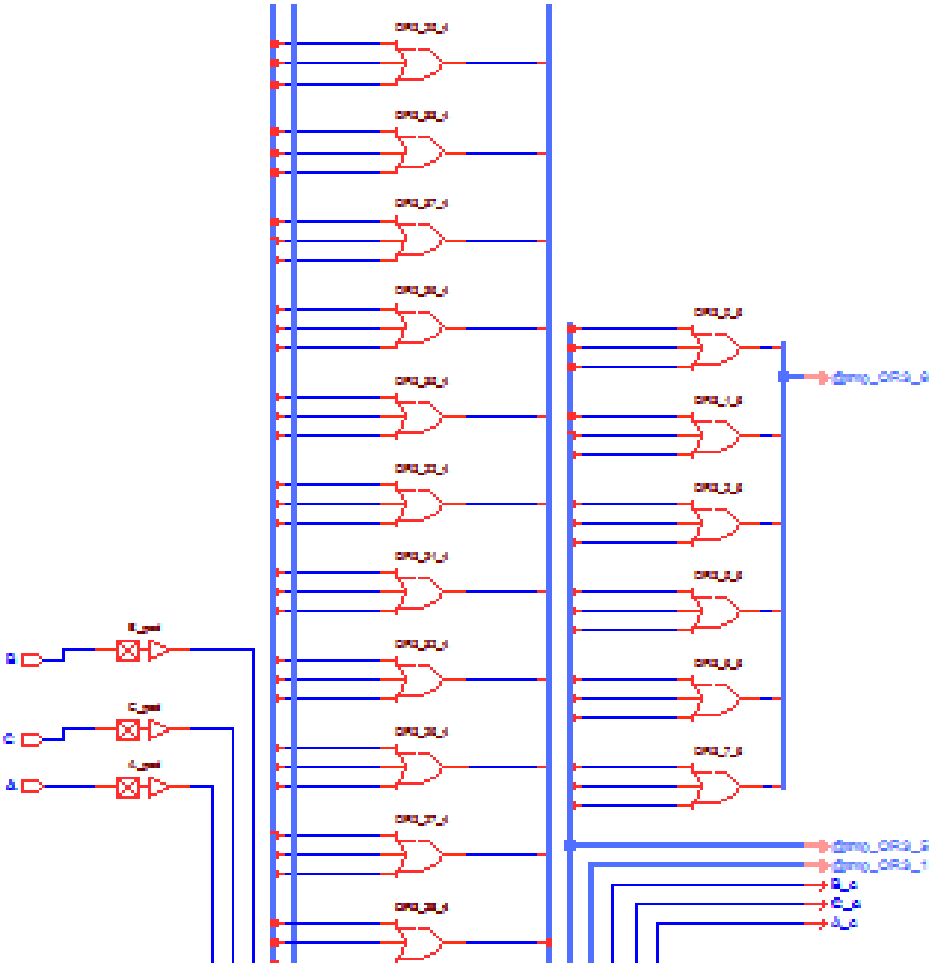

Figure 23:OR column schematic

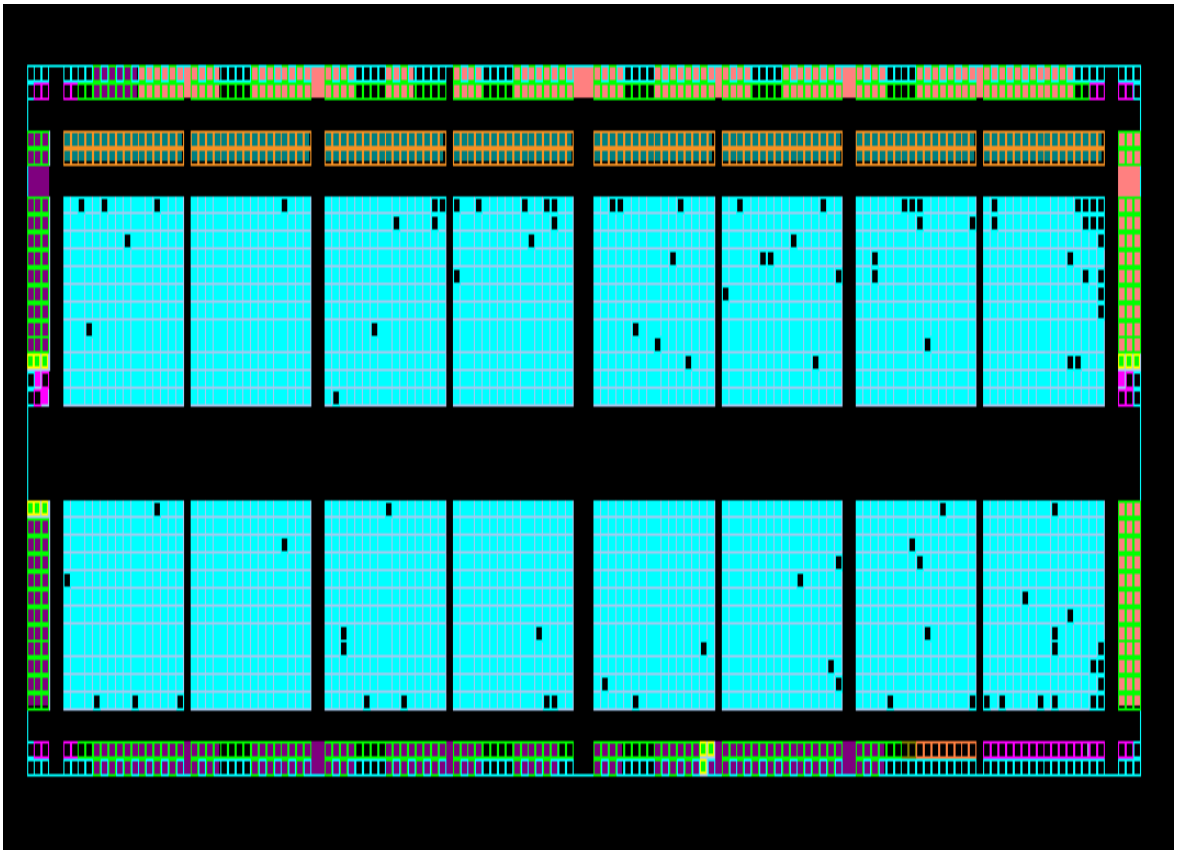

Figure 24:Leakage current experiment layout

9.6 Experiment result

After irradiation the FPGA chip and measuring the leakage current at the input pins for all the input combinations unfortunately no current could be measured. This happened for all the levels of radiation dose with two different chips. The reason for this might be the input buffers which are made from CMOS circuits, while those buffers leak at high ionization dose. At high ionization dose the effect of the leakage current from floating gate transistors will not have any significance and no point to be compared with CMOS leakage current.

Chapter 10

CONCLUSION AND FUTURE WORK

As a focus on delay failures induced in flash-based FPGAs due to total ionizing dose. The failure analysis indicated that delay failure is caused by degradation introduced by the floating gate switches along the delay path. The work developed a fault model for the delay failure. Using this model, the worst-case condition for the delay failure is the path that has the maximum number of floating gate switches. The work developed a novel search methodology for worst-case test vectors that uses both static timing analyses as well as search algorithms. The work finally compared the delay failure level for three cases: worst, nominal, and best, which clarifies the significance of using worst-case conditions in total dose testing of FPGAs.

More investigation about the application of this fault model on larger design could be very useful and also designing a CAD tool specialized for applying the fault model on any design to get the worst case test vectors.

Continuing the leakage current fault model following the same steps presented in this thesis for the propagation delay fault model is a good point to be done whenever there is a facility to measure the input current at the nodes just after the input buffers.

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